REMARKS

CLAIMS

The Applicants respectfully submit that the Examiner does not show a teaching of each and every element recited in the pending claims. Consequently, the Examiner should withdraw the rejections made to the pending claims. Furthermore, the Examiner has not clearly pointed out how each and every element is taught or disclosed by the cited references. For example, the Examiner alleges that she shows a teaching by referencing one or more large sections of text in a cited reference without specifically pointing out or logically explaining how each element or feature is taught using the cited references. Applicants would appreciate it if the Examiner would provide the specific words or phrases within the cited references which may be used to teach an element and/or feature of a claim. Furthermore, the Applicants believe that the Examiner has not responded to Applicants' arguments made in the Response dated August 15, 2007 since she restates what was previously stated in the Office Action dated May 16, 2007. Also, it appears the Examiner replicates arguments to various claims without providing a specific response to a claim.

As was stated in the interview with the Applicants' representative on January 18, 2007, the Examiner had indicated that the feature "reducing the size of a translation lookaside buffer" had not been given patentable weight since it was recited in the preamble of Claim 1. Therefore, in the request for continued examination (RCE), the Applicants incorporated this patentable feature into Claims 29, 32, and 35 seeking allowance of these claims. However, to the Applicants' disbelief, the Examiner has subsequently rejected Claims 29, 32, and 35 by providing flawed reasoning in the Office Actions. For example, the Examiner has repeatedly referenced physical register 0 (element 106) and physical register 1 (element 104), at Col. 6,

lines 55-58, and at Figure 3, of Hinton, in her attempt to show a teaching of "reducing the size of a translation lookaside buffer." However, this passage or any other passage in Hinton, does not teach any method or system that reduces the size of a buffer, as recited in several of the pending claims. Hinton merely uses a bit to select from two different registers (i.e., physical register 0 (element 106) and physical register 1 (element 104)) in a buffer (i.e., Hinton's translation write buffer (TWB)), which does not disclose any reduction in memory size in comparison to what is recited in Claims 29, 32, and 35, for example. Therefore, Hinton does not teach or disclose a method or system that reduces the size of a translation lookaside buffer. Therefore, the Examiner has not demonstrated a teaching of at least this patentable feature recited in Claims 29, 32, and 35. Applicants request allowance of Claims 29, 32, and 35 along with their corresponding dependent claims.

The Examiner wishes to use a TWB (translation write buffer) in Hinton to teach a TLB (translation lookaside buffer) providing write *and read* functionality (emphasis denoted in italics), in the manner recited in one or more method and system claims (e.g., independent Claims 18, 21, 32, 35). The Applicants have repeatedly stated that the cited reference (Hinton) does not disclose a TLB providing read functionality as recited in these claims since Hinton does not teach or disclose each and every element that is recited in these claims. The Examiner fails to show a teaching of how Hinton's TWB provides read functionality as recited in these claims. The Examiner's complete response, as found on page 22 of the last Office Action is to simply state that "Hinton expressly discloses a ["Mini-TLB (TWB)," defined as "A small 3-entry instruction mini TLB (6)" (Columns 5-6, lines 62-67 and 1-5)]; therefore, TWB is a TLB of reduced/mini size." Furthermore, the Applicants have examined Cols. 5-6, lines 62-67 and 1-5, but have not found any disclosure of the read functionality recited in Claims 21, 32, and 35, for

example. For example, the Applicants request that the Examiner specifically point how *each and every element* of "b) reading said page frame number data from said single page frame number field, said first storage register used to read said page frame number data when said bit is said first value, said second storage register used to read said page frame number data when said bit is said second value, said bit used to reduce size of said translation lookaside buffer by way of consolidating two page frame number fields of said indexed entry into a single page frame number field" is taught or disclosed by Examiner's cited reference (i.e., Hinton). Applicants believe that the Examiner has failed to address Applicants' arguments. Applicants request that the Examiner specifically point out (using specific and direct evidence from the reference, without large portions of text) how *each and every element* is taught by Hinton.

Furthermore, the Examiner has not shown a teaching of "consolidating even and odd page frame numbers into *a single page frame number field*," as recited in Claim 12 (emphasis denoted in italics), as the Applicants have examined and thoroughly reviewed Examiner's cited passages in Hinton (i.e., Hinton, at Col. 6, lines 37-63 or Col. 7, lines 5-14, and/or Figure 3). Likewise, nowhere is there a teaching of "a buffer that uses a single page frame number field for storing odd/even page frame numbers," as recited, for example, in Claim 16. The Applicants respectfully request the Examiner show a teaching of each and every element and/or feature of Claims 12 and 16. Applicants respectfully submit that the Examiner has not shown a teaching of patentable subject matter as recited in at least independent Claims 12, 16, 18, 21, 29, 32, 35, and 41. Therefore, these independent claims and their associated dependent claims should be passed to allowance.

REMARKS TO EXAMINER'S POINTS OF ARGUMENT

In pages 22-27 of the current Office Action dated October 29, 2007, the Examiner makes an attempt to support her three points of argument she originally made in the non-final Office Action dated May 16, 2007. In the Response dated August 15, 2007, the Applicants had addressed and challenged these points to show that the Examiner had not shown a teaching of the pending claims. In the current Office Action, the Examiner has not responded to the Applicants' arguments in the Response dated August 15, 2007. Therefore, the Applicants feel that the Examiner has been unable to clearly and logically show a teaching of the patentable subject matter recited in the pending claims.

1st POINT OF ARGUMENT

The Office Action states:

> 33. Regarding Applicant's remark that Hinton's translation write buffer (TWB) does not teach a translation lookaside buffer (TLB) as Hinton's TWB comprises elements that are functionally different from Applicant's claimed invention; the Examiner would like to point out that Hinton discloses the invention as required by the claims **[See rejection to claims above].**
>
> Furthermore, Hinton expressly discloses **["Mini-TLB (TWB)," defined as "A small 3-entry instruction mini TLB (6)" (Columns 5-6, lines 62-67 and 1-5)]; therefore, TWB is a TLB of reduced/mini size.**
>
> 34. Regarding Applicant's remark that the TWB disclosed by Hinton performs only write operations and not reading and writing as required by the claims; the Examiner disagrees as Hinton discloses **["the logical registers in the TWB compare bits 13 to 31 of this logical address with their stored values 204. If they compare, it is a TWB hit (206). The control logic selects one of these**

> **register's hit signals, depending on the value of logical address bit 12 (208)" (Col. 7, lines 25-25)** ***(which comprises reading from the TWB; which corresponds to Applicant's claimed TLB)*** **wherein if the instruction is a TWB miss, "then the TWB stores away the logical and physical address in one of its entries (232). This is the mechanism by which the TWB is loaded" (Figure 7 and related text)** ***(which comprises writing into the TWB; which corresponds to Applicant's claimed TLB)]. Hinton also explains "first and second logical registers in said TWB resulting in a first hit signal with respect to said first logical register or a second hit signal with respect to said second logical register... F. gating to a physical address bus a stored value in one of said first or second physical address registers associated with said selected hit signal*** **(which comprises reading from on of the registers of TWB, as claimed)...** ***issuing a machine bus fetch, upon a condition that said upper order bits of said logical address do not equal a stored value in said first or second logical register in said TWB;... M storing in said TWB said logical address and said second physical address upon a condition that said lower order bits are identical*** **(which comprises writing into one of the registers TWB, as claimed)"** ***(Col. 7, line 54-Col. 8; line 45).***

See Office Action at pages 22-23.

In response to item #33, the Examiner has not provided any specific response to Applicants' arguments concerning the patentability of Claims 12 and 18, as she merely requests the Applicants to "see rejection to claims above," without providing any specific evidence that shows a teaching of the elements recited in these claims. Applicants had clearly demonstrated that Hinton's TWB is functionally different from a translation lookaside buffer (TLB) as recited in the claimed invention. Furthermore, Hinton's registers are not the same as the mini-TLB registers disclosed in the claimed invention. As supported by the specification of the present Application, the mini-TLB registers are located outside of the translation lookaside buffer (mini-

TLB). The Examiner states that Hinton discloses "reading from on(e) [sic] of the registers of (Hinton's) TWB, as claimed." However, the Examiner is incorrect, since the claimed invention does not recite registers within a buffer. For example, Hinton does not teach the "first storage register" and "second storage register," as recited in Claim 18 because Hinton's registers are contained within a buffer (i.e., the TWB). Furthermore, the Examiner is requested to review the supporting specification, at Figure 3, which clearly illustrates the relationship of the claimed translation lookaside buffer (TLB) and the registers. As illustrated in Figure 3, the TLB does not comprise the registers. Hence, the Examiner does not show a teaching of what is recited in at least Claim 18, for example. Likewise, the Examiner does not show a teaching of the pending claims. Therefore, the pending claims should be passed to allowance.

The Applicants respectfully submit that two sets of physical registers as disclosed in Hinton do not teach "a method of improving the performance of address translation in a TLB comprising using a bit obtained from a virtual page number to indicate whether a page frame number is even or odd; and consolidating even and odd page frame number fields into a single page frame number field of said translation lookaside buffer," as recited in Claim 12, for example. Therefore, for this reason alone, the Examiner has not shown a teaching of each and every element of what is recited in Claim 12.

Examiner's next remark is to merely state that a *small* buffer may be used to teach the TLB recited in the pending claims. Applicants do not see how merely referencing "a small 3-entry instruction mini TLB" shows a teaching of what is recited in Claim 12. Applicants respectfully submit that this does not show a teaching of what is recited in Claim 12.

With respect to item #34, Applicants do not see how a TWB hit teaches the process of "reading and writing odd and even page frame numbers using a single page frame number field"

as recited in claim 18. As the Applicants have restated in a number of instances, Hinton does not disclose anything about "reading and writing odd and even page frame numbers using a single page frame number field." Thus, for this reason alone, the Examiner has not shown a teaching of each and every element of what is recited in Claim 18. Furthermore, the Applicants request the Examiner to *specifically* show how Hinton may be used to teach the second and third clauses of what is recited in Claim 18 (emphasis denoted in italics). Applicants request the Examiner to show a teaching of each and every element of "a first register for mapping an even page frame number to said single page frame number field; and a second register for mapping an odd page frame number to said single page frame number field." If the Examiner is unable to do so, Claim 18 should be passed to allowance.

Overall, the Examiner has not provided a proper examination of the pending claims. The Examiner is requested to fully consider the arguments made by the Applicants with regard to the subject matter recited in the pending claims. After considering the arguments presented by the Applicants, the Examiner is asked to clearly and logically show a teaching of *each and every element* recited in the pending claims (emphasis denoted in italics). For example, the Examiner does not provide any cohesive argument when she references a rather large portion of text in Hinton, at Col. 7, line 54 – Col. 8, line 45 while attempting to show a teaching of what is recited in Claims 12, 16, 18, and 21. Therefore, for at least the foregoing reasons, the Applicants believe that the pending claims contain patentable subject matter.

2ND POINT OF ARGUMENT

The Office Action states:

35. Regarding Applicant's argument that Hinton does not disclose storing even

and odd page frame numbers into a single page frame number field of said translation lookaside buffer as Hinton discloses two separate registers; this argument has been considered and is not persuasive.

First of all, the Examiner would like to point out that Applicant's Specification describes storing even and odd page frame numbers into a single page frame number field of said translation lookaside buffer as **["Figure 3 is a relational block diagram illustrating an organizational structure of a mini-TLB system 300 in accordance with an embodiment of the invention. The mini-TLB system 300 comprises a miniature version of the previously mentioned translation lookaside buffer described in Figure 1 (herein termed a mini-TLB 304) communicating with a number of mini-TLB registers 308 and a control processor 324.**

In one embodiment, the mini-TLB 304 is configured by way of instructions executed by the control processor 324. For the mini-TLB 304 shown in Figure 3, the index and page mask registers function in the same manner as was described earlier in Figure 1. In addition, virtual addressing is performed using the addressing format described in Figure 2, in which a 32 bit virtual address is used. Of course, it is contemplated that in other embodiments, virtual addressing may be performed using more or less than 32 bits. In the embodiment shown, the entry Hi 312 register of Figure 3 facilitates storage and read out of a virtual page number associated with bits [31:12] of the virtual addressing format discussed previously. Hence, as illustrated in Figure 3, the virtual page number (VPN) may be either read from or written into a VPN field (or section) 316 of the mini-TLB 304. The VPN is associated with a page frame number (PFN) which is similarly either read from or written into a PFN field 320 of the mini-TLB 304 using the registers shown (i.e., entry Lo0 or entry Lo1 registers). In the embodiment illustrated in Figure 3, only one of the entry Lo registers (either entry Lo0 or entry Lo1) is valid for use during a write operation; for example, the contents of a valid entry Lo register is written. into the page frame number (PFN)

field 320 associated with a specified page table entry of the mini-TLS 304. In one embodiment, the least significant bit (lsb) of a VPN (i.e., bit 12 of the 32 bit virtual address described) is used to determine whether the entry Lo0 or an entry Lol register contains valid data for writing into the PFN field 320 of the mini-TLB 304. Similar principles may be applied during a read from the mini-TLB 304. For example, the least significant bit (lsb) of the VPN may be used to determine which register, either entry Lo0 or entry Lol, will be used to access valid page frame number data utilized by the control processor 324 during a read operation. In a read operation, for example, the least significant bit (lsb) of a virtual page number is used to store data into either the entry Lo0 register or the entry Lol register. In this fashion, both even and odd page frame numbers may be stored or recalled from a single page frame number field of the mini-TLB 304" (Applicant's Specification, Paragraph 0026)1. Therefore, Applicant's Specification discloses two registers and reading/writing to only one of these two registers when reading/writing to TLB. Emphasis added on underlined portions.

Hinton discloses this limitation as **["Mini-TLB (TWB)," defined as "A small 3-entry instruction mini TLB (6)" (Columns 5-6, lines 62-67 and 1-5) to provide access to memory wherein "the instruction pointer is comprised of logical address bits including upper order bits, lower order bits, and a single bit having a first value or a second value, the single bit providing for translation of even-number pages for which the single bit has a first value and for odd-number pages for which the single bit has the second value" (Columns 1-2, lines 64-67 and 1-29; Column 6, lines 37-63; Figure 3) "`TWB" (mini TLB) (Figure 3, Diagram of TWB) in which "a logical address (81) is separated into three parts... Bit 12 selects which of the two entries in the TWB are to be used for this address... Registers (106) marked "0" are for even-numbered 4KB pages, addresses for which bit 12 is a zero. Registers (104) marked "1" are for odd-numbered 4KB pages, addresses for which bit 12 is a one" (Column 6, lines 37-63) wherein for a TWB load, "one**

set (even or odd) of the TWB registers in loaded with the logical and physical addresses" (Column 7, lines 5-14). ***Hinton also explains "first and second logical registers in said TWB resulting in a first hit signal with respect to said first logical register or a second hit signal with respect to said second logical register... F. gating to a physical address bus a stored value in one of said first or second physical address registers associated with said selected hit signal*** **(which comprises reading from on of the registers of TWB, as claimed)..,** ***issuing a machine bus fetch, upon a condition that said upper order bits of said logical address do not equal a stored value in said first or second logical register in said TWB;... M storing in said TWB said logical address and said second physical address upon a condition that said lower order bits are identical*** **(which comprises writing into one of the registers TWB, as claimed)"** ***(Col. 7, line 54-Col. 8; line 45).***

Therefore, even logical and physical address set is read from/written to TWB and odd logical and physical address set are read from/written to TWB. Therefore, Hinton discloses writing and reading even and odd page frame numbers into a single page frame number field".

For example, when bit 12 is a 0, TWB (Translation Write Buffer or mini-TLB) will read and write in a single field within Physical Register.0 (which is used for even pages), which comprises reading and writing even page frame numbers into a single page frame number field of a translation lookaside buffer. For further explanation, when bit 12 is a 1, TWB will read and write into a single field within Physical Register 1 (which is used for odd pages), which comprises reading and writing odd page frame numbers into a single page frame number field. Therefore, Hinton discloses, "writing and reading even and odd page frame numbers into a single page frame number field" of a translation lookaside buffer, as claimed by Applicant).

See Office Action at pages 23-27.

While the Examiner makes an attempt to show a teaching of what is disclosed in Applicants' specification, the Examiner has not shown a teaching of what is recited in the

pending claims. The Examiner restates sections of the Applicants' specification and Hinton without providing a coherent argument. The Examiner states that **"Therefore, even logical and physical address set is read from/written to TWB and odd logical and physical address set are read from/written to TWB. Therefore, Hinton discloses writing and reading even and odd page frame numbers into a single page frame number field."** Applicants do not see how Examiner's conclusion is reached that she shows a teaching of what is recited in the claims. The Applicants respectfully disagree that Hinton teaches "using a bit of a virtual page number of a virtual address for reading and writing odd and even page frame numbers using a single page frame number field of said translation lookaside buffer," as recited in Claim 18 for example. Furthermore, nowhere does Hinton disclose anything about "using a single page frame number field," for example. The Examiner has not disclosed any verbiage in Hinton that can be used to show a teaching of what is recited in Claim 18. Applicants wonder how a physical register in a TWB may be used to show a teaching of the recited feature in Claim 18 when the claimed invention does not recite a physical register. Therefore, the Examiner has failed to show a teaching of each and every element in Claim 18.

As indicated in the preceding passage, the first part of the Examiner's response is to recite pages 10-11 of Applicants' specification. Paragraph 26 and Figure 3 of the specification discloses a translation lookaside buffer (i.e., a mini-TLB) communicating with a number of mini-TLB registers 308. As clearly shown in Figure 3**, the mini-TLB does not comprise the mini-TLB registers (i.e., the mini-TLB registers are not inside (or within) the mini-TLB)**. In an attempt to show a teaching, it appears that the Examiner wishes to map two physical registers within a buffer (Hinton's translation write buffer) to two registers outside of a buffer (translation lookaside buffer of the claimed invention). The Examiner wishes to teach the translation

lookaside buffer (mini-TLB) recited in the pending claims by way of using Hinton's registers (elements 104, 106, Figure 3, Hinton). However, the Examiner does not realize that Hinton's registers do not teach the translation lookaside buffer recited in the claimed invention. As supported in the specification, the mini-TLB registers are not located within the translation lookaside buffer (i.e., mini-TLB). Consequently, for this reason alone, the Applicants respectfully submit that the Examiner has not shown a teaching of the translation lookaside buffer recited in the pending claims.

Perhaps the Examiner should refer back to pages 14-15, in the previous Response dated August 15, 2007. Furthermore, perhaps the Examiner should review the Applicants' remarks at the following section of the current Response: DEPENDENT CLAIMS 15, 17, AND 19, AND INDEPENDENT CLAIMS 29, 32, AND 35. Hinton does not teach, disclose, or suggest a method and/or system that reduces the size of a buffer. For example, Hinton does not teach, disclose, or suggest a method to "reduce the size of said translation lookaside buffer" as recited in Claim 32. The two physical registers (elements 104, 106) within Hinton's TWB, as disclosed in Hinton at Figure 3, for example, do not teach the translation lookaside buffer (TLB) recited in the pending claims since the two registers claimed are not contained within the claimed translation lookaside buffer. The two physical registers (within a TWB) disclosed by Hinton are different from "a first register for mapping an even page frame number to said single page frame number field; and a second register for mapping an odd page frame number to said single page frame number field," as recited in Claim 18. Applicants do not see how the mere use of two physical registers could possibly be used to teach a method to "reduce the size of a translation lookaside buffer," as recited in Claim 18, for example. As was stated in the 1st Point of Argument, the Examiner has again referenced the text in Hinton, at Col. 7, line 54 – Col. 8, line

45. However, the Examiner does not provide any cohesive argument when referencing this rather large portion of text. Therefore, for at least the foregoing reasons, Claims 12, 16, and 18, as well as any pending claims that recite this feature should be allowed.

3RD POINT OF ARGUMENT

The Office Action states:

> 36. In response to Applicant's remark that Hinton does not disclose reducing the size of the TLB; the Examiner disagrees and submits that Hinton discloses this limitation as **["Mini-TLB (TWB)," defined as "A small 3-entry instruction mini TLB (6)" (Columns 5-6, lines 62-67 and 1-5) which is of mini/reduced size. Applicant should note that by using "a single bit having a first value or a second value, the single bit providing for translation of even-number pages for which the single bit has a first value and for odd-number pages for which the single bit has the second value" (Columns 1-2, lines 64-67) wherein even-number pages will only be written within "physical register 0 - 106" and odd-number pages will only be written within "physical register 1 - 104;" therefore, having a single entry for each page depending on the value of bit 12 and implementing a TLB of reduced size or mini- TLB, as claimed (See Figures 3 an d 7 and related text)].**

See Office Action at page 27.

Applicants respectfully submit that the Examiner has not considered Applicants' previous remarks and/or arguments because the Examiner continues to make the same argument without responding to Applicants' arguments. In fact, the Examiner's response is exactly the same as her previous response for this section. Therefore, the Applicants respectfully request the Examiner to refer to Applicants' response in pages 15-16 of the Response dated August 15, 2007, which states:

As a third point of Applicants' argument, the Office Action has improperly characterized and/or interpreted what is disclosed in Hinton. For example, at the first paragraph of page 4 of the Office Action dated 5/16/07, the Examiner states that "Therefore, only an even or an odd logical and physical address set (which corresponds to the claimed page frame number) is loaded (which comprises reading or writing) on TWB (which corresponds to the claimed translation lookaside buffer)." Firstly, nowhere does Claim 12 or Claim 16 or Claim 18 recite anything about an even or odd logical and physical address set. Thus, for this reason alone, the Examiner has not shown a teaching of what is recited each of Claims 12, 16, and 18. Secondly, Hinton does not disclose anything about a page frame number or page frame number field as recited in Claims 12, 16, and 18. Thus, for each of these reasons alone, Hinton does not teach what is recited in Claims 12, 16, and 18; as a consequence, Claims 12, 16, and 18 contain patentable subject matter and should be allowed. The Examiner interprets the term "loaded" to mean "reading or writing" in an attempt to teach a translation lookaside buffer (TLB) recited in Claims 12 and 18. Applicants respectfully disagree that the term "loaded" is equivalent to the term "reading or writing." Therefore, the Applicants respectfully submit that for this reason alone, the Examiner has not shown a teaching of what is recited in Claims 12 and 18. Because of each of the foregoing reasons, the Office Action does not show a teaching of what is recited in Claims 12, 16, and 18.

As was stated previously, Applicants believe that the Office Action has improperly characterized what is disclosed in Hinton. Applicants do not find any disclosure in Hinton of "an even or an odd logical and physical address set." Secondly, even if there is disclosure of such an address set, Applicants fail to see how this would teach anything about a page frame number or a (single) page frame number field as recited in Claims 12, 16, and 18. For at least the foregoing

reasons, the Applicants believe that at least Claims 12, 16, and 18 contain patentable subject matter. Therefore, Applicants request allowance of at least these claims.

REJECTION OF CLAIMS 12-23, 25, 29-34 AND 41-43 UNDER 35 U.S.C. § 102(b)

Claims 12-23, 25, 29-34 and 41-43 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,500,948 ("Hinton").

INDEPENDENT CLAIMS 12, 16 AND 18

Regarding Claims 12, 16 and 18, the Office Action restates what was stated in the non-final Office Action dated May 16, 2007, except for the portion indicated in italics:

> As per **claims 12, 16 and 18,** Hinton discloses a method/system of improving the performance of address translation in a translation lookaside buffer comprising using a bit obtained from a virtual page number to indicate whether a page frame number is even or odd; and consolidating even and odd page frame number fields into a single page frame number field of said translation lookaside buffer;
>
> virtual to physical memory address translation comprising a buffer that uses a single page frame number field for storing odd/even page frame numbers comprising: a translation lookaside buffer, said translation lookaside buffer using a bit of a virtual page number of a virtual address for reading and writing odd and even page frame numbers using a single page frame number field of said translation lookaside buffer; a first register for mapping an even page frame number to said single page frame number fields; and a second register for mapping an odd page frame number to said single page frame number field
>
> as ["**Mini-TLB (TWB)," defined as "A small 3-entry instruction mini TLB (6)" (Columns 5-6, lines 62-67 and 1-5) to provide access to memory wherein "the instruction pointer is comprised of logical address bits**

including upper order bits, lower order bits, and a single bit having a first value or a second value, the single bit providing for translation of even-number pages for which the single bit has a first value and for odd-number pages for which the single bit has the second value" (Columns 1-2, lines 64-67 and 1-29; Column 6, lines 37-63; Figure 3) "TWB" (mini TLB) (Figure 3, Diagram of TWB) in which "a logical address (81) is separated into three parts... Bit 12 selects which of the two entries in the TWB are to be used for this address... Registers (106) marked "0" are for even-numbered 4KB pages, addresses for which bit 12 is a zero. Registers (104) marked "1" are for odd-numbered 4KB pages, addresses for which bit 12 is a one" (Column 6, lines 37-63) wherein for a TWB load, "one set (even or odd) of the TWB registers in loaded with the logical and physical addresses" (Column 7, lines 5-14). ***Hinton also explains "first and second logical registers in said TWB resulting in a first hit signal with respect to said first logical register or a second hit signal with respect to said second logical register... F. gating to a physical address bus a stored value in one of said first or second physical address registers associated with said selected hit signal... issuing a machine bus fetch, upon a condition that said upper order bits of said logical address do not equal a stored value in said first or second logical register in said TWB;... M storing in said TWB said logical address and said second physical address upon a condition that said lower order bits are identical" (Col. 7, line 54-Col. 8; line 45).*** **Therefore, only an even or an odd logical and physical address set (which corresponds to the claimed page frame number) is loaded (which comprises reading or writing) on TWB (which corresponds to the claimed translation lookaside buffer). Therefore, Hinton discloses writing and reading even and odd page frame numbers into a single page frame number field".**

For example, when bit 12 is a 0, TWB (Translation Write Buffer or mini-TLB) will read and write in a single field within Physical Register 0 (which is used for even pages), which comprises reading and writing even

> **page frame numbers into a single page frame number field of a translation lookaside buffer. For further explanation, when bit 12 is a 1, TWB will read and write into a single field within Physical Register 1 (which is used for odd pages), which comprises reading and writing odd page frame numbers into a single page frame number field. Therefore, Hinton discloses, "writing and reading even and odd page frame numbers into a single page frame number field" c f a translation lookaside buffer, as claimed by Applicant].**

See Office Action at pages 2-4.

Claim 12 recites "A method of improving the performance of address translation in a translation lookaside buffer comprising: using a bit obtained from a virtual page number to indicate whether a page frame number is even or odd; and consolidating even and odd page frame number fields into a single page frame number field of said translation lookaside buffer."

Claim 16 recites "A system to provide effective virtual to physical memory address translation comprising a buffer that uses a single page frame number field for storing odd/even page frame numbers."

Claim 18 recites "A system to provide virtual to physical memory address translation of a translation lookaside buffer comprising: a translation lookaside buffer, said translation lookaside buffer using a bit of a virtual page number of a virtual address for reading and writing odd and even page frame numbers using a single page frame number field of said translation lookaside buffer; a first register for mapping an even page frame number to said single page frame number field; and a second register for mapping an odd page frame number to said single page frame number field."

The Applicants maintain the arguments that were previously presented in the Response dated August 15, 2007 with respect to Claims 12, 16, and 18. Therefore, the Applicants

respectfully request the Examiner to refer to the Applicants' arguments presented in the Response dated August 15, 2007.

With respect to the newly presented remarks made by the Examiner (as indicated in italics), the Applicants do not see how this verbiage (which is simply an excerpt from Hinton, at Col. 7, line 54 – Col. 8, line 45) shows a teaching of what is recited in any one of Claims 12, 16, and 18. Further, the Examiner has failed to provide a logical explanation as to how this excerpt from Hinton may be used to show a teaching of any one of Claims 12, 16, and 18. Thus, the Examiner alleges that she shows a teaching by referencing one or more large sections of text in a cited reference without specifically pointing out or logically explaining how a word or phrase within a large section of text teaches what is recited in a claim. The Applicants respectfully submit that the Examiner has not made an attempt to clearly and specifically point out how the verbiage of Hinton, at Col. 7, line 54 – Col. 8, line 45, teaches what is recited in any one of Claims 12, 16, and 18. Furthermore, the Examiner has failed to provide any sort of argument that addresses the new elements and/or features incorporated into Claims 12 and 18. For example, the Examiner has failed to show a teaching of "using a bit obtained from a virtual page number to indicate whether a page frame number is even or odd." Furthermore, for example, the Examiner has failed to show a teaching of "a first register for mapping an even page frame number to said single page frame number field; and a second register for mapping an odd page frame number to said single page frame number field," as recited in Claim 18. Therefore, for at least all of these reasons, the Applicants respectfully submit that independent Claims 12, 16, and 18 contain patentable subject matter, and that these claims should be passed to allowance. Applicants respectfully request allowance of independent Claims 12, 16, and 18.

The Applicants respectfully submit that because of the foregoing reasons, independent Claims 12, 16 and 18 contain patentable subject matter and should be allowed. As a result of providing the foregoing arguments with respect to independent Claims 12, 16 and 18, the Applicants may not have commented on all the remarks made by the Examiner regarding dependent Claims 13-15, 17 and 19-20 but reserve the right to do so in the future should the need arise. Since Claims 13-15, 17 and 19-20 depend on allowable Claims 12, 16 and 18, respectively, Applicants respectfully submit that Claims 13-15, 17 and 19-20 are also in condition for allowance. Thus, the Applicants respectfully request that Claims 12-20 be allowed.

DEPENDENT CLAIMS 15, 17, AND 19, AND INDEPENDENT CLAIMS 29, 32, AND 35

As was stated previously by the Applicants in the beginning remarks of this Response with respect to independent Claims 29, 32, and 35, the Examiner has referenced Hinton, physical register 0 (element 106) and physical register 1 (element 104), at Figure 3, in her attempt to show a teaching of implementing a reduced size translation lookaside buffer. However, the Applicants do not see any disclosure by Hinton, of reducing the size of a translation lookaside buffer, since Hinton discloses a bit used to select from two different registers (i.e., physical register 0 (element 106) and physical register 1 (element 104)) located within a buffer (Hinton's translation write buffer (TWB)). Thus, Hinton does not teach or disclose a method or system that reduces the size of a buffer. Therefore, the Applicants respectfully submit that the Examiner's argument is flawed. Since Claims 15, 17, 19, 29, 32, and 35 describe reducing the size of a translation lookaside buffer by using a single page frame number field (as opposed to two page frame number fields), the Examiner's reference to a physical register 0 (element 106) and a physical register 1 (element 104) at Col. 6, lines 55-58, and at Figure 3 of Hinton does not teach what is

recited in these claims. Therefore, the Examiner has not provided any disclosure from Hinton that teaches what is recited in Claims 15, 17, 19, 29, 32, and 35. Consequently, the Applicants request allowance of these claims. Applicants respectfully request allowance of dependent Claims 30-31, 33, and 36-40 since they depend on allowable independent Claims 29, 32, and 35, respectively.

INDEPENDENT CLAIM 21

Regarding Claim 21, the Office Action states:

> As per **claim 21** (new), Hinton discloses A method of implementing a reduced size translation lookaside buffet comprising:
>
> obtaining a bit obtained from a virtual page number of a virtual address;
>
> using said bit to determine which one of two storage registers will be used for:
>
> a) writing page frame number data from said one of two registers into an indexed entry of a single page frame number field of said translation lookaside buffer, said two storage registers comprising a first storage register used for writing even page frame numbers into said single page frame number field when said bit is a first value and a second storage register used for writing odd page frame numbers into said single page frame number field when said bit is a second value, **or** b) reading said page frame number data from said single page frame number field, said first storage register used to read said page frame number data when said bit is said first value, said second storage register used to read said page frame number data when said bit is a second value, said bit used to reduce size of said translation lookaside buffer by way of consolidating two page frame number fields of said indexed entry into a single page frame number field **[Hinton discloses "the instruction pointer is comprised of logical address bits" (Col. 2, lines 9-10) which corresponds to Applicant's claimed page number wherein "a logical address (81) is separated into three parts... Bit 12 selects**

which of the two entries in the TWB are to be used for this address... Registers (106) marked "0" are for even-numbered 4KB pages, addresses for which bit 12 is a zero. Registers (104) marked "1" are for odd-numbered 4KB pages, addresses for which bit 12 is a one" (Column 6, lines 37-63) wherein for a TWB load, "one set (even or odd) of the TWB registers in loaded with the logical and physical addresses" (Column 7, lines 5-14) and Figure 3 and explains "the logical registers in the TWB compare bits 13 to 31 of this logical address with their stored values 204. If they compare, it is a TWB hit (206). The control logic selects one of these register's hit signals, depending on the value of logical address bit 12 (208)" (Col. 7, lines 25-25) ***(which comprises reading from the TWB; which corresponds to Applicant's claimed TLB)*** **wherein if the instruction is a TWB miss, "then the TWB stores away the logical and physical address in one of its entries (232). This is the mechanism by which the TWB is loaded" (Figure 7 and related text) [wherein if the instruction is a TWB miss, "then the TWB stores away the logical and physical address in one of its entries (232). This is the mechanism by which the TWB is loaded" (Figure 7 and related text)** ***(which comprises writing into the TWB; which corresponds to Applicant's claimed TLB)*** **wherein "registers (106) marked "0" are for even-numbered 4KB pages, addresses for which bit 12 is a zero. Registers (104) marked "1" are for odd-numbered 4KB pages, addresses for which bit 12 is a one" (Col. 6, lines 56-59)]. ["the logical registers in the TWB compare bits 13 to 31 of this logical address with their stored values 204. If they compare, it is a TWB hit (206). The control logic selects one of these register's hit signals, depending on the value of logical address bit 12 (208)" (Col. 7, lines 25-25)** ***(which comprises reading/retrieving from the TWB; which corresponds to Applicant's claimed TLB)*** **wherein "registers (106) marked "0" are for even-numbered 4KB pages, addresses for which bit 12 is a zero. Registers (104) marked "1" are for odd-numbered 4KB pages, addresses for which bit 12 is a one" (Col. 6, lines 56-59)]** ***(which comprises writing into the TWB; which corresponds to***

Applicant's claimed TLB)].[sic]

Hinton also explains "first and second logical registers in said TWB resulting in a first hit signal with respect to said first logical register or a second hit signal with respect to said second logical register... F. gating to a physical address bus a stored value in one of said first or second physical address registers associated with said selected hit signal **(which comprises reading from on of the registers of TWB, as claimed)...** ***issuing a machine bus fetch, upon a condition that said upper order bits of said logical address do not equal a stored value in said first or second logical register in said TWB; ... M storing in said TWB said logical address and said second physical address upon a condition that said lower order bits are identical*** **(which comprises writing into one of the registers TWB, as claimed)"** ***(Col. 7, line 54-Col. 8; line 45).***

Hinton discloses **["Mini-TLB (TWB)," defined as "A small 3-entry instruction mini TLB (6)" (Columns 5-6, lines 62-67 and 1-5) which is of mini/reduced size. Applicant should note that by using "a single bit having a first value or a second value, the single bit providing for translation of even-number pages for which the single bit has a first value and for odd-number pages for which the single bit has the second value" (Columns 1-2, lines 64-67) wherein even-number pages will only be written within "physical register 0 - 106" and odd-number pages will only be written within "physical register 1 - 104;" therefore, having a single entry for each page depending on the value of bit 12 and implementing a TLB of reduced size or mini-TLB, as claimed (See Figures 3 and 7 and related text)].**

For example, when bit 12 is a 0, TWB (Translation Write Buffer or mini-TLB) will read and write in a single field within Physical Register 0 (which is used for even pages), which comprises reading and writing even page frame numbers into a single page frame number field of a translation lookaside buffer. For further explanation, when bit 12 is a 1, TWB will read and write into a single field within Physical Register 1 (which is used for odd pages), which comprises reading and writing odd page frame numbers into a

single page frame number field. Therefore, Hinton discloses, "writing and reading even and odd page frame numbers into a single page frame number field" of a translation lookaside buffer, as claimed by Applicant].

See Office Action at pages 6-9.

Claim 21 recites "A method comprising: obtaining a bit obtained from a virtual page number of a virtual address; using said bit to determine which one of two storage registers will be used for: a) writing page frame number data from said one of two storage registers into an indexed entry of a single page frame number field of said translation lookaside buffer, said two storage registers comprising a first storage register used for writing even page frame numbers into said single page frame number field when said bit is a first value and a second storage register used for writing odd page frame numbers into said single page frame number field when said bit is a second value, or b) reading said page frame number data from said single page frame number field, said first storage register used to read said page frame number data when said bit is said first value, said second storage register used to read said page frame number data when said bit is said second value, said bit used to reduce size of said translation lookaside buffer by way of consolidating two page frame number fields of said indexed entry into a single page frame number field."

Since much of what the Examiner states with respect to Claims 12, 16, and 18 is restated with respect to Claim 21, it is evident that the Examiner merely repeats the same argument she makes for other claims. With respect to Claim 21, the Applicants respectfully request that the Examiner review Applicants' arguments that were previously presented in pages 19-21 of the Response dated August 15, 2007. Furthermore, none of the Examiner's arguments logically addresses and/or responds to Applicants' arguments made in the previous Response dated August 15, 2007. It is clear that the Examiner has not shown a teaching of each and every

element recited in Claim 21. Unless the Examiner clearly and specifically points out how each element of Claim 21 is disclosed by Hinton, the Applicants maintain that Claim 21 contains patentable subject matter, that should be allowed.

In the last paragraph of the above passage obtained from the Office Action at pages 6-9, the Examiner has significantly characterized what is disclosed in Hinton. For example, nowhere does Hinton disclose a "page frame number" as the Examiner has stated. Furthermore, nowhere does Hinton disclose "*reading and writing even page frame numbers into a single page frame number field*" as the Examiner has stated. Nowhere is there any disclosure of this in Hinton. Applicants respectfully request the Examiner to refrain from characterizing what is disclosed in Hinton in an attempt to show a teaching of Claim 21. The Applicants respectfully submit that Hinton does not teach what is recited in Claim 21. Furthermore, the Examiner does not teach each and every element and/or feature recited in Claim 21. For example, the Examiner does not teach "reading said page frame number data from said single page frame number field, said first storage register used to read said page frame number data when said bit is said first value, said second storage register used to read said page frame number data when said bit is said second value, said bit used to reduce size of said translation lookaside buffer by way of consolidating two page frame number fields of said indexed entry into a single page frame number field," as recited in Claim 21. For example, Hinton does not teach "writing page frame number data from said one of two storage registers into an indexed entry of a single page frame number field," as recited in Claim 21.

Therefore, for at least the foregoing reasons, the Office Action has not shown a teaching of what is recited in Claim 21. Thus, Claim 21 contains patentable subject matter.

Consequently, the Applicants respectfully submit that the patentable subject matter in Claim 21 should be advanced to allowance.

The Applicants respectfully submit that because of the foregoing reasons, independent Claim 21 contains patentable subject matter and should be allowed. As a result of providing the foregoing arguments with respect to independent Claim 21, the Applicants may not have commented on all the remarks made by the Examiner regarding dependent Claims 22-28 but reserve the right to do so in the future should the need arise. Since Claims 22-28 depend on allowable Claim 21, Applicants respectfully submit that Claims 22-28 are in condition for allowance. The Applicants respectfully request allowance of Claims 21-28.

INDEPENDENT CLAIM 29

Regarding Claim 29, the Office Action states:

> As per **claim 29** (new), Hinton discloses A method of performing a write operation using a translation lookaside buffer comprising:
>
> using a bit of a virtual page number, said virtual page number stored in a data register; assessing whether a value of said bit of a virtual page number is 0 or 1; translating a first page frame number stored in a first register to a page frame number field of an indexed entry of said translation lookaside buffer if said value is 0; and writing a second page frame number stored in a second register to said page frame number field of said indexed entry of said translation lookaside buffer if said value is 1, **[Hinton discloses "the instruction pointer is comprised of logical address bits" (Col. 2, lines 9-10) which corresponds to Applicant's claimed page number wherein "a logical address (81) is separated into three parts... Bit 12 selects which of the two entries in the TWB are to be used for this address... Registers (106) marked "0" are for even-numbered 4KB pages, addresses for which bit 12 is a zero. Registers (104) marked "1" are**

for odd-numbered 4KB pages, addresses for which bit 12 is a one" (Column 6, lines 37-63) wherein for a TWB load, "one set (even or odd) of the TWB registers in loaded with the logical and physical addresses" (Column 7, lines 5-14) and Figure 3 and explains "the logical registers in the TWB compare bits 13 to 31 of this logical address with their stored values 204. If they compare, it is a TWB hit (206). The control logic selects one of these register's hit signals, depending on the value of logical address bit 12 (208)" (Col. 7, lines 25-25) ***(which comprises reading from the TWB; which corresponds to Applicant's claimed TLB)*** **wherein if the instruction is a TWB miss, "then the TWB stores away the logical and physical address in one of its entries (232). This is the mechanism by which the TWB is loaded" (Figure 7 and related text)** ***(which comprises writing into the TWB; which corresponds to Applicant's claimed TLB)]***

said indexed entry, comprising a single page frame number field used to reduce the size of said translation lookaside buffer **[With respect to this limitation, Hinton discloses "Mini-TLB (TWB)," defined as "A small 3-entry instruction mini TLB (6)" (Columns 5-6, lines 62-67 and 1-5). Applicant should note that by using "a single bit having a first value or a second value, the single bit providing for translation of even-number pages for which the single bit has a first value and for odd-number pages for which the single bit has the second value" (Columns 1-2, lines 64-67) wherein even-number pages will only be written within "physical register 0 - 106" and odd-number pages will only be written within "physical register 1 - 104;" therefore, having a single entry for each page depending on the value of bit 12 and implementing a TLB of reduced size, as claimed (See Figures 3 and 7 and related text)].**

See Office Action at pages 10-11.

Claim 29 recites "A method of performing a write operation using a translation lookaside buffer comprising: using a bit of a virtual page number, said virtual page number stored in a data register; assessing whether a value of said bit of a virtual page number is 0 or 1; writing a first

page frame number stored in a first register to a page frame number field of an indexed entry of said translation lookaside buffer if said value is 0; and writing a second page frame number stored in a second register to said page frame number field of said indexed entry of said translation lookaside buffer if said value is 1, said indexed entry comprising a single page frame number field used to reduce the size of said translation lookaside buffer."

The Examiner has restated the same argument she made in the previous Office Action. Therefore, the Applicants maintain the arguments that were previously presented in the Response dated August 15, 2007 with respect to Claim 29. Therefore, the Applicants respectfully request the Examiner to refer to the Applicants' arguments presented in the Response dated August 15, 2007. Furthermore, the Applicants request the Examiner to refer to Applicants' previously made arguments for dependent Claims 15, 17, and 19 and independent Claims 29, 32, and 35. For these reasons, Claims 29, 32, and 35 contain patentable subject matter, which should be allowed.

Applicants respectfully submit that the Office Action does not show a teaching of "using a bit of a virtual page number," as recited in Claim 29. For at least this reason, the Applicants respectfully submit that Claim 29 contains patentable subject matter. Furthermore, nowhere does Hinton's invention teach an "indexed entry comprising a single page frame number field used to reduce the size of said translation lookaside buffer," as recited in Claim 29. The Applicants respectfully submit that Hinton does not teach what is recited in Claim 29. Therefore, for at least these reasons, the Office Action has not shown a teaching of what is recited in Claim 29. Thus, Claim 29 contains patentable subject matter. Consequently, the Applicants respectfully submit that the patentable subject matter in Claim 29 should be advanced to allowance.

The Applicants respectfully submit that because of the foregoing reasons, independent Claim 29 contains patentable subject matter and should be allowed. As a result of providing the

foregoing arguments with respect to independent Claim 29, the Applicants may not have commented on all the remarks made by the Examiner regarding dependent Claims 30-31 but reserve the right to do so in the future should the need arise. Since Claims 30-31 depend on allowable Claim 29, Applicants respectfully submit that Claims 30-31 are in condition for allowance. The Applicants respectfully request that Claims 29-31 be allowed.

INDEPENDENT CLAIM 32

Regarding Claim 32, the Office Action states:

> As per **claim 32** (new) A method of performing a read operation using a translation lookaside buffer comprising:
>
> using a bit of a virtual page number, said virtual page number stored in virtual page number field of said translation lookaside buffer; assessing whether n value of a bit of a virtual page number is 0 or 1; reading a page frame number stored in a page flame number field of an indexed entry of said translation 10okaside [sic] buffer, storing said page frame number into a first register if said value is 0; and storing said page frame number into a second register if said value is 1, said indexed entry comprising a single page frame number field used to reduce the size of said translation lookaside buffer **[The rationale in the rejection to claim 29 is herein incorporated].**

See Office Action at page 12.

Claim 32 recites "A method of performing a read operation using a translation lookaside buffer comprising: using a bit of a virtual page number, said virtual page number stored in virtual page number field of said translation lookaside buffer; assessing whether a value of a bit of a virtual page number is 0 or 1; reading a page frame number stored in a page frame number field of an indexed entry of said translation lookaside buffer; storing said page frame number into a first register if said value is 0; and storing said page frame number into a second register if said

value is 1, said indexed entry comprising a single page frame number field used to reduce the size of said translation lookaside buffer."

The Examiner has restated the same argument she made in the previous Office Action. Therefore, the Applicants maintain the arguments that were previously presented in the Response dated August 15, 2007 with respect to Claim 32. The Applicants respectfully request the Examiner to refer to the Applicants' arguments presented in the Response dated August 15, 2007. Furthermore, the Applicants request the Examiner to refer to Applicants' previously made arguments for dependent Claims 15, 17, and 19 and independent Claims 29, 32, and 35. For these reasons, Claims 29, 32, and 35 contain patentable subject matter, which should be allowed.

Applicants respectfully submit that the Office Action does not show a teaching of "using a bit of a virtual page number," as recited in Claim 32. For at least this reason, the Applicants respectfully submit that Claim 32 contains patentable subject matter. Furthermore, nowhere does Hinton's invention teach an "indexed entry comprising a single page frame number field used to reduce the size of said translation lookaside buffer," as recited in Claim 32. Therefore, for this reason alone, the Office Action has not shown a teaching of what is recited in Claim 32. Thus, Claim 32 contains patentable subject matter. Consequently, the Applicants respectfully submit that the patentable subject matter in Claim 32 should be advanced to allowance.

The Applicants respectfully submit that because of the foregoing reasons, independent Claim 32 contains patentable subject matter and should be allowed. As a result of providing the foregoing arguments with respect to independent Claim 32, the Applicants may not have commented on all the remarks made by the Examiner regarding dependent Claim 33 but reserve the right to do so in the future should the need arise. Since Claim 33 depends on allowable

Claim 32, Applicants respectfully submit that Claim 33 is in condition for allowance. The Applicants respectfully request that Claims 32-33 be allowed.

INDEPENDENT CLAIM 34

Regarding Claim 34, the Office Action states:

> As per **claim 34** (new) A method of probing for a particular virtual page number of an entry in a translation lookaside buffer comprising:
>
> using a virtual page number stored in a first register; comparing said virtual page number to one or more values stored in one or more virtual page number fields of one or more corresponding entries in said translation lookaside buffer; generating an identifying number associated with an entry of said one or more entries if a virtual page number field stores a value that is equal to said virtual page number; and storing said identifying number into a second register **["Mini-TLB (TWB)," defined as "A small 3-entry instruction mini TLB.(6)" (Columns 5-6, lines 62-67 and 1-5) to provide access to memory wherein "the instruction pointer is comprised of logical address bits including upper order bits, lower order bits, and a single bit having a first value or a second value, the single bit providing for translation of even-number pages for which the single bit has a first value and for odd-number pages for which the single bit has the second value" (Columns 1-2, lines 64-67 and 1-29; Column 6, lines 37-63; Figure 3) "TWB" (mini TLB) (Figure 3, Diagram of TWB) in which "a logical address (81) is separated into three parts... Bit 12 selects which of the two entries in the TWB are to be used for this address... Registers (106) marked "0" are for even-numbered 4KB pages, addresses for which bit 12 is a zero. Registers (104) marked "1" are for odd-numbered 4KB pages, addresses for which bit 12 is a one" (Column 6, lines 37-63) wherein for a TWB load, "one set (even or odd) of the TWB registers in loaded with the logical and physical addresses" (Column 7, lines 5-14). Therefore, only an even or an odd logical and physical address set (which corresponds to the**

> **claimed page frame number) is loaded (which comprises reading or writing) on TWB (which corresponds to the claimed translation lookaside buffer). Therefore, Hinton discloses writing and reading even and odd page frame numbers into a single page frame number field.**
>
> For example, when bit 12 is a 0, TWB (Translation Write Buffer or mini-TLB) will read and write in a single field within Physical Register 0 (which is used for even pages), which comprises reading and writing even page frame numbers into a single page frame number field of a translation lookaside buffer. For further explanation, when bit 12 is a 1, TWB will read and write into a single field within Physical Register 1 (which is used for odd pages), which comprises reading and writing odd page frame numbers into a single page frame number field. Therefore, Hinton discloses, "writing and reading even and odd page frame numbers into a single page frame number field" of a translation lookaside buffer, as claimed by Applicant] [See figure 7 and related text].

See Office Action at pages 12-13.

Claim 34 recites "A method of probing for a particular virtual page number of an entry in a translation lookaside buffer comprising: using a virtual page number stored in a first register; comparing said virtual page number to one or more values stored in one or more virtual page number fields of one or more corresponding entries in said translation lookaside buffer; generating an identifying number associated with an entry of said one or more entries if a virtual page number field stores a value that is equal to said virtual page number; and storing said identifying number into a second register."

The Examiner has restated the same argument she made in the previous Office Action. Therefore, the Applicants maintain the arguments that were previously presented in the Response dated August 15, 2007 with respect to Claim 34. Therefore, the Applicants respectfully request

the Examiner to refer to the Applicants' arguments presented in the Response dated August 15, 2007.

Applicants respectfully submit that the Office Action does not show a teaching of "using a virtual page number stored in a first register," as recited in the first clause of Claim 34. For at least this reason, the Applicants respectfully submit that Claim 34 contains patentable subject matter. Applicants respectfully submit that the Office Action does not show a teaching of "comparing said virtual page number to one or more values stored in one or more virtual page number fields of one or more corresponding entries in said translation lookaside buffer," as recited in the second clause of Claim 34. For at least this reason, the Applicants respectfully submit that Claim 34 contains patentable subject matter. Applicants respectfully submit that the Office Action does not show a teaching of "generating an identifying number associated with an entry of said one or more entries if a virtual page number field stores a value that is equal to said virtual page number, and storing said identifying number into a second register," as recited in the third and fourth clauses of Claim 34. Thus, Claim 34 contains patentable subject matter. Consequently, the Applicants respectfully submit that the patentable subject matter in Claim 34 should be advanced to allowance.

INDEPENDENT CLAIM 41

Regarding Claim 41, the Office Action states:

> As per claim 41. (New) A reduced size translation lookaside buffer comprising: a virtual page number field used to store a virtual page number; a page frame number field used to store an even or an odd page frame number, said even or said odd page frame number indicated by a bit from said virtual page number **[The rationale in the rejection to claim 21 is herein incorporated].**

See Office Action at pages 13-14.

Claim 41 recites "A reduced size translation lookaside buffer comprising: a virtual page number field used to store a virtual page number; a page frame number field used to store an even or an odd page frame number, said even or said odd page frame number indicated by a bit from said virtual page number."

The Examiner's argument for Claim 41 merely states that "the rationale in the rejection to claim 21 is herein incorporated." The Applicants believe that the Examiner has been unable to show a teaching of what is recited in Claim 21. The Applicants respectfully submit that, among other things, the Examiner has not shown a teaching of Claim 41 since Claim 21 does not recite a "virtual page number field." Thus, for at least this reason alone, Claim 41 contains patentable subject matter. Consequently, the Applicants request allowance of Claim 41.

As a result of providing the foregoing arguments with respect to independent Claim 41, the Applicants may not have commented on all the remarks made by the Examiner regarding dependent Claims 42-43 but reserve the right to do so in the future should the need arise. Since Claims 42-44 depend on allowable Claim 41, Applicants respectfully submit that Claims 42-44 are in condition for allowance. The Applicants respectfully request allowance of Claims 41-44.

REJECTION OF CLAIMS 35-38 AND 40 UNDER 35 U.S.C. § 103(a)

Claims 35-38 and 40 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Hinton.

INDEPENDENT CLAIM 35

Regarding Claim 35, the Office Action states:

As per **claim 35** (new), AAPA discloses A translation lookaside buffer system comprising: a translation lookaside buffer; **["TLB 104" (Applicant's Specification; Figure 1 and related text)]**

a first register used for storing a value that indexes an entry in said translation lookaside buffer, said entry comprising a virtual page number field and a single page frame number field; **["index 132" (Applicant's Specification; Figure 1 and related text)]**

a second register used for storing a page size of said entry; **["page mask 136" (Applicant's Specification; Figure 1 and related text)]**

a third register used for storing a virtual page number of said entry, said virtual page number comprising a bit; **["Entry Hi" (Applicant's Specification; Figure 1 and related text)]**

a fourth register used for storing an even page frame number; **["entry Loo" (Applicant's Specification; Figure 1 and related text)]**

and a fifth register used for storing an odd page frame number, **["entry Lol" (Applicant's Specification; Figure 1 and related text)].**

AAPA does not disclose expressly said bit of said virtual page number used to determine whether said even page frame number or said odd page flame number is to be stored in said page frame number field in said translation lookaside buffer when performing a write operation, said bit of said virtual page number stored in said virtual page number field used to determine whether said even page flame number is to be stored in said fourth register or ~aid **[sic]** odd page frame number is' **[sic]** to be stored in said fifth register when performing a read operation, wherein use of said single page frame number field reduces the size of said translation lookaside buffer.

Hinton discloses said bit of said virtual page number used to determine whether said even page frame number or said odd page flame number is to be stored in said page frame number field in said translation lookaside buffer when performing a write operation, said bit of said virtual page number stored in said virtual page number field used to determine whether said even page flame number

is to be stored in said fourth register or ~aid **[sic]** odd page frame number is' **[sic]** to be stored in said fifth register when performing a read operation, wherein use of said single page frame number field reduces the size of said translation lookaside buffer as **[Hinton discloses "the instruction pointer is comprised of logical address bits" (Col. 2, lines 9-10) which corresponds to Applicant's claimed page number wherein "a logical address (81) is separated into three parts... Bit 12 selects which of the two entries in the TWB are to be used for this address... Registers (106) marked "0" are for even-numbered 4KB pages, addresses for which bit 1-2 is a zero. Registers (104) marked "1" are for odd-numbered 4KB pages, addresses for which bit 12 is a one" (Column 6, lines 37-63) wherein for a TWB load, "one set (even or odd) of the TWB registers in loaded with the logical and physical addresses" (Column 7, lines 5-14) and Figure 3 and explains "the logical registers in the TWB compare bits 13 to 31 of this logical address with their stored values 204. If they compare, it is a TWB hit (206). The control logic selects one of these register's hit signals, depending on the value of logical address bit 12 (208)" (Col. 7, lines 25-25) *(which comprises reading from the TWB; which corresponds to Applicant's claimed TLB)* wherein if the instruction is a TWB miss, "then the TWB stores away the logical and physical address in one of its entries (232). This is the mechanism by which the TWB is loaded" (Figure 7 and related text) *(which comprises writing into the TWB; which corresponds to Applicant's claimed TLB)* wherein "Mini-TLB (TWB)," defined as "A small 3-entry instruction mini TLB (6)" (Columns 5-6, lines 62-67 and 1-5). Applicant should note that by using "a single bit having a first value or a second value, the single bit providing for translation of even-number pages for which the single bit has a first value and for odd-number pages for which the single bit has the second value" (Columns 1-2, lines 64-67) wherein even-number pages will only be written within "physical register 0 - 106" and odd-number pages will only be written within "physical register 1 - 104;" therefore, having a single entry for each page depending on the value of bit**

12 and implementing a TLB of reduced size, as claimed (See Figures 3 and 7 and related text)].

Applicant Admitted Prior Art (AAPA) and Hinton et al. (US 5,500,948) are analogous art because they are from the same field of endeavor of computer memory access and control.

At the time of the invention it would have beers obvious to a person of ordinary skill in the art to modify the TLB system as taught by APPA and further said bit of said virtual page number used to determine whether said even page frame number or said odd page flame number is to be stored in said page frame number field in said translation lookaside buffer when performing a write operation, said bit of said virtual page number stored in said virtual page number field used to determine whether said even page flame number is to be stored in said fourth register or said odd page frame number is' **[sic]** to be stored in said fifth register when performing a read operation, wherein use of said single page frame number field reduces the size of said translation lookaside buffer as taught by Hinton.

The motivation for doing so would have been because Hinton discloses **["it is an object of the present invention to provide an address translation mechanism that will translate a logical address from a program counter to a physical address to be used to check an on-chip cache for an instruction" (Col. 1, lines 57-60) for efficient address translation].**

Therefore, it would have been obvious to combine Applicant Admitted Prior Art (AAPA) with Hinton et al. (US 5,500,948) for the benefit of creating a translation lookaside buffer to obtain the invention as specified in claims 35.

See Office Action at pages 16-19.

Claim 35 recites "A translation lookaside buffer system comprising: a translation lookaside buffer; a first register used for storing a value that indexes an entry in said translation lookaside buffer, said entry comprising a virtual page number field and a single page frame number field; a second register used for storing a page size of said entry; a third register used for

storing a virtual page number of said entry, said virtual page number comprising a bit; a fourth register used for storing an even page frame number; and a fifth register used for storing an odd page frame number, said bit of said virtual page number used to determine whether said even page frame number or said odd page frame number is to be stored in said page frame number field in said translation lookaside buffer when performing a write operation, said bit of said virtual page number stored in said virtual page number field used to determine whether said even page frame number is to be stored in said fourth register or said odd page frame number is to be stored in said fifth register when performing a read operation, wherein use of said single page frame number field reduces the size of said translation lookaside buffer."

The Examiner has restated the same argument she made in the previous Office Action. Therefore, the Applicants maintain the arguments that were previously presented in the Response dated August 15, 2007 with respect to Claim 35. The Applicants respectfully request the Examiner to refer to the Applicants' arguments presented in the Response dated August 15, 2007. Furthermore, the Applicants request the Examiner to refer to Applicants' previously made arguments for dependent Claims 15, 17, and 19 and independent Claims 29, 32, and 35. For these reasons, Claims 29, 32, and 35 contain patentable subject matter, which should be allowed.

The Applicants respectfully submit that Hinton does not teach what is recited in Claim 35. For example, the Office Action does not show a teaching of "wherein use of said single page frame number field reduces the size of said translation lookaside buffer." Therefore, for this reason alone, the Office Action has not shown a teaching of what is recited in Claim 35. Thus, Claim 35 contains patentable subject matter. Consequently, the Applicants respectfully submit that the patentable subject matter in Claim 35 should be advanced to allowance.

The Applicants respectfully submit that because of the foregoing reasons, independent Claim 35 contains patentable subject matter and should be allowed. As a result of providing the foregoing arguments with respect to independent Claim 35, the Applicants may not have commented on all the remarks made by the Examiner regarding dependent Claims 36-40 but reserve the right to do so in the future should the need arise. Since Claims 36- 40 depend on allowable Claim 35, Applicants respectfully submit that Claims 36-40 are in condition for allowance. The Applicants respectfully request allowance of Claims 35-40.

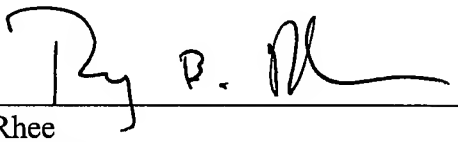
CONCLUSION

Based on at least the foregoing, the Applicants believe that Claims 12-44 are in condition for allowance. A Notice of Allowance is courteously solicited. Should anything remain in order to place the present Application in condition for allowance, or should the Examiner disagree or have any question regarding this submission, the Examiner is kindly invited to contact the undersigned at (312) 775-8246.

The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to the Deposit Account of McAndrews, Held & Malloy, Ltd., Account No. 13-0017.

Dated: December 19, 2007

Respectfully submitted,



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